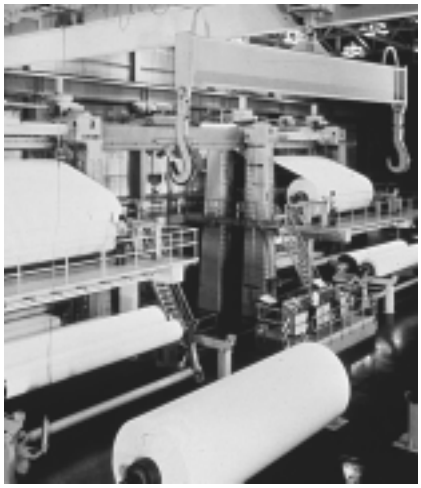
SLC 500™ Chassis–Based Processors

(Catalog Numbers 1747–L511, –L514, –L524, –L531, –L532, –L541, –L542, –L543, –L551, –L552, –L553)

Product Data



The SLC 500 product line allows you to build just the right control system to meet your needs. We offer four chassis sizes, five power supplies, eleven processors, and a wide variety of I/O modules. Additionally, we offer flexible communication options and programming and operator interface options.

The SLC 500 family of programmable controllers have expanded to meet a broader range of applications. From high–speed packaging and material handling applications to advanced process control applications, Allen–Bradley offers the right processor for your job.

The SLC 5/03™ , SLC 5/04™ and SLC 5/05™ processors offer features previously found only on high–level Plus. The SLC 500 processors provide a broad range of communication options, including DH–485, RS–232, DH+™, and Ethernet™. Increased instruction support with ASCII, floating point math, and indirect addressing allows you to expand your application's capabilities.

Publication 1747-2.39

Features and Benefits

Supports user memory sizes from 1K to 64K. By offering a wide range of user memory, SLC 500 modular processors can be used in a wide variety of applications.

Supports a variety of input and output modules. The 1746 modular I/O system offers over 60 types of modules, allowing you to customize your control solution to meet your application needs.

Supports I/O configurations of up to 3 chassis (30 local I/O slots). Provides you with the flexibility to expand I/O capacity as required.

Supports remote I/O and DeviceNet. The SLC 5/02 and above processors support up to 4096 discrete inputs and 4096 discrete outputs which may be a mix of local or remote I/O as well as I/O on DeviceNet.

Provides superior system throughput. SLC 500 modular processors deliver fast overall system throughput times, providing fast response in high–speed applications.

Supports Ethernet communication. The SLC 5/05 processors support 10 Mbps Ethernet communication and use the TCP/IP protocol. The 10Base–T Ethernet channel provides an economical connection to your Ethernet network.

Supports Data Highway Plus™ (DH+) communication. The SLC 5/04 processor provides communication and seamless integration into the larger Allen–Bradley PLC–5® network.

Supports DH–485 communication. Communication via the DH–485 network is available in every processor we ship, reducing your system cost for processor communication.

Provides a second channel for RS–232 communication for the SLC 5/03, SLC 5/04, and SLC 5/05 processors. This allows:

- dial up for remote monitoring and programming
- networking over modems for SCADA master/slave RTU applications
- an alternate connection for operator interfaces freeing up peer–to–peer network
- direct communication to ASCII devices such as bar code decoders and serial printers via a complete set of ASCII ladder instructions which simplify programming.

Provides user–selectable program security. The wide range of system protection capabilities allow you to secure user data and program files from changes.

Supports a host of third–party products through the Allen–Bradley Encompass Program. The Encompass Program provides access to products and services that increase your application capabilities.

Overview of the Processors

The SLC 500 processor product line offers five types of chassis–based processors.

SLC 5/01™ Processor (Catalog # 1747–L511 or 1747–L514)

The SLC 5/01 processor offers the instruction set of the SLC 500 fixed controller in a modular hardware configuration. The SLC 5/01 processor provides:

- two choices of program memory size - 1K or 4K instructions
- control of up to 3840 input and output points
- powerful ladder logic programming instruction set
- subroutines
- a DH–485 communication channel (peer–to–peer communication response to message commands only)
- capacitor backup for the –L511; battery backup for the –L514

SLC 5/02™ Processor (Catalog # 1747–L524)

The SLC 5/02 processor offers additional instructions, increased diagnostics, faster throughput, and additional peer–to–peer communication options; building on what the SLC 5/01 processors offer. The SLC 5/02 processor provides:

- program memory size of 4K instructions
- control of up to 4096 input and output points
- PID - used to provide closed loop process control
- indexed addressing
- interrupt capability
- user fault routines
- ability to handle 32–bit signed math functions
- built–in DH–485 communication channel (initiation of peer–to–peer communication)
- battery–backed RAM

SLC 5/03™ Processor (Catalog # 1747–L531 and 1747–L532)

The SLC 5/03 processor significantly increases performance by supplying system throughput times of 1 ms for a typical 1K user program. Now applications such as high–speed packaging, sorting, and material handling become more affordable. With the addition of online editing, the SLC 5/03 processor presents a positive solution for your continuous process application. A built–in RS–232 channel gives you the flexibility to connect to external intelligent devices without the need for additional modules. The SLC 5/03 processor provides:

- program memory size of 8K or 16K
- control of up to 4096 input and output points
- online programming (includes runtime editing)
- built–in DH–485 channel
- built–in RS–232 channel, supporting:
  - — DF1 Full–Duplex for point–to–point communication; remotely via a modem, or direct connection to programming or operator interface devices. (Use a 1747–CP3 cable for direct connection.)
  - — DF1 Half–Duplex Master/Slave for SCADA type (point–to–multipoint) communication
  - — DH–485 (Serves as a second DH–485 channel. Use a 1761–NET–AIC with a 1747–CP3 cable to connect to the DH–485 network.)
  - — ASCII I/O for connection to other ASCII devices, such as bar code readers, serial printers, and weigh scales
- remote I/O passthru
- built–in real–time clock/calendar
- 2 ms Selectable Timed Interrupt (STI)
- 0.50 ms Discrete Input Interrupt (DII)
- advanced math features - trigonometric, PID, exponential, floating point, and the compute instruction
- indirect addressing
- flash PROM provides firmware upgrades without physically changing EPROMS
- optional flash EPROM memory module available
- keyswitch - RUN, REMote, PROGram (clear faults)
- battery–backed RAM

SLC 5/04™ Processor (Catalog # 1747–L541, –L542, or –L543)

The SLC 5/04 processor provides the baseline functionality of the SLC 5/03 processor plus DH+ communication. Communication via DH+ takes place 3 to 12 times faster than DH–485, providing you with increased performance levels. In addition, the SLC 5/04 processor runs approximately 15% faster than the SLC 5/03 processor. The SLC 5/04 processor provides:

- program memory sizes of 16K, 32K, or 64K
- high–speed performance - 0.90 ms/K typical
- control of up to 4096 input and output points
- online programming (includes runtime editing)
- built–in DH+ channel, supporting:
  - — high–speed communication (57.6K, 115.2K, and 230.4K baud)
  - — messaging capabilities with SLC 500, PLC–2®, PLC–5®, and PLC–5/250 processors
- built–in RS–232 channel, supporting:
  - — DF1 Full–Duplex for point–to–point communication; remotely via a modem, or direct connection to programming or operator interface devices. (Use a 1747–CP3 cable for direct connection.)
  - — DF1 Half–Duplex Master/Slave for SCADA type (point–to–multipoint) communication
  - — DH–485 (Use a 1761–NET–AIC with a 1747–CP3 cable to connect to the DH–485 network.)
  - — ASCII I/O for connection to other ASCII devices, such as bar code readers, serial printers, and weigh scales
- channel–to–channel (DH+ to DH–485) passthru capability to operator interface devices
- channel–to–channel (DF1 Full–Duplex to DH+) passthru (OS401 and later only)
- remote I/O passthru
- built–in real–time clock/calendar
- 1 ms Selectable Timed Interrupt (STI)
- 0.50 ms Discrete Input Interrupt (DII)
- advanced math features - trigonometric, PID, exponential, floating point, and the compute instruction
- indirect addressing
- flash PROM provides firmware upgrades without physically changing EPROMS
- optional flash EPROM memory module available
- keyswitch - RUN, REMote, PROGram (clear faults)
- battery–backed RAM

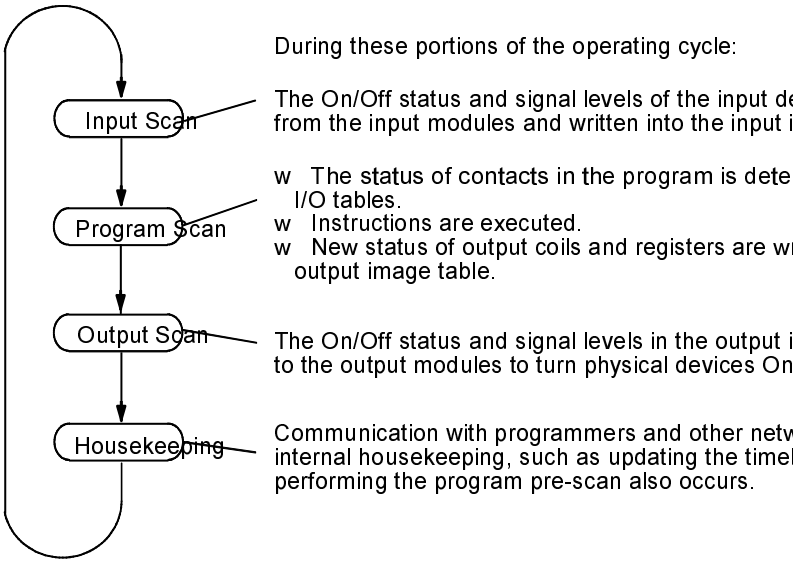
SLC 5/05™ Processor (Catalog # 1747–L551, –L552, or –L553)

The SLC 5/05 processor provides identical functionality as the SLC 5/04 processor using standard Ethernet communications. Ethernet communication takes place at 10 Mbps, providing you with a high performance network for program upload/download, on–line editing, and peer–to–peer messaging. The variety of memory sizes allows you to closely match your application needs. The SLC 5/05 provides:

- program memory sizes of 16K, 32K, or 64K
- high–speed performance - 0.90 ms/K typical
- control of up to 4096 input and output points
- online programming (includes runtime editing)
- built–in 10Base–T Ethernet channel, supporting:
  - — high–speed computer communication using TCP/IP
  - — messaging capabilities with SLC 5/05, PLC–5, and PLC–5/250 processors, 1785–ENET Ethernet interface module, and 1756–ENET Ethernet bridge
  - — SNMP for standard Ethernet network management
  - — BOOTP for optional dynamic IP address assignment
- built–in RS–232 channel, supporting:
  - — DF1 Full–Duplex for point–to–point communication; remotely via a modem, or direct connection to programming or operator interface devices. (Use a 1747–CP3 cable for direct connection.)
  - — DF1 Half–Duplex Master/Slave for SCADA type (point–to–multipoint) communication
  - — DH–485 (Use a 1761–NET–AIC with a 1747–CP3 cable to connect to the DH–485 network.)
  - — ASCII I/O for connection to other ASCII devices, such as bar code readers, serial printers, and weigh scales
- remote I/O passthru
- built–in real–time clock/calendar
- 1 ms Selectable Timed Interrupt (STI)
- 0.50 ms Discrete Input Interrupt (DII)
- advanced math features - trigonometric, PID, exponential, floating point, and the compute instruction
- indirect addressing
- logical ASCII addressing
- flash PROM provides firmware upgrades without physically changing EPROMS
- optional flash EPROM memory module available
- keyswitch - RUN, REMote, PROGram (clear faults)
- battery–backed RAM

System Throughput

When your application requires high–speed processing it requires more than just fast instruction or program scan times. It requires speed from the time an input is read until the time an output is turned on. The SLC 500 processors improve performance in every phase of system throughput, from input and output scans, to program scans and housekeeping functions.



Interrupt Subroutines

The following interrupt subroutines allow you to provide predetermined responses to special events in an application.

Selectable Timed Interrupt

This function allows you to interrupt the scan of the processor automatically, on a periodic basis, in order to scan a specified subroutine file. When using an SLC 5/02 processor, the Selectable Timed Interrupt (STI) timebase can be adjusted in 10 ms increments. The timebase for the SLC 5/03, SLC 5/04, and SLC 5/05 processors can be adjusted in 1 ms increments. The SLC 5/03 processor begins at 2 ms STI, and the SLC 5/04 and SLC 5/05 processors begin at 1 ms STI.

Discrete Input Interrupt

Use the Discrete Input Interrupt (DII) for high–speed processing applications or any application that needs to respond to an event quickly. This function allows the processor to execute a ladder subroutine when the input bit pattern of a discrete I/O card matches a compare value that you programmed. The discrete input interrupt is examined every 100 µs asynchronous to the ladder program scan. You may also specify the number of counts (matches) to occur before subroutine execution.

I/O Event Interrupt

This function allows the 1746–BAS (BASIC) module to interrupt the normal processor operating cycle in order to scan a specified subroutine file. Use this interrupt with SLC 5/02, SLC 5/03, SLC 5/04, and SLC 5/05 processors.

Communication Options

The SLC 500 processors support different types of communication options. The following sections describe the physical connections and protocol options used by the processors.

Physical Connection Options

Ethernet (10Base–T) channel offers:

- 10 Mbps communication rate
- ISO/IEC 8802–3STD 802.3 (RJ45) connector for 10Base–T media
- TCP/IP communication protocol
- built–in isolation

Data Highway Plus (DH+) channel offers:

- communication rates of 57.6K, 115.2K, and 230.4K baud
- maximum network length of 3,048 m (10,000 ft.) at 57.6K baud
- Belden 9463 (blue hose) cable connection between nodes (daisy chain connection)
- built–in isolation

DH–485 channel offers:

- configurable communication rates up to 19.2K baud
- electrical isolation via the 1747–AIC or 1761–NET–AIC
- maximum network length of 1219m (4,000 ft.)
- RS–485 electrical specifications
- Belden 9842 or Belden 3106A cable connection between nodes (daisy chain connection)

RS–232 channel offers:

- communication rates up to 19.2K baud (38.4K baud SLC 5/05)
- maximum distance between devices is 15.24 m (50 ft.)
- RS–232C (EIA–232) electrical specifications
- modem support
- built–in isolation

The table below summarizes the SLC 500 processor channel connections.

Processor		Physical Communication Channel			
		DH-485	RS-232[a]	DH+	Ethernet
SLC 5/01		DH-485 protocol			
SLC 5/02		DH-485 protocol			
SLC 5/03	Channel 0		DH-485, DF1 Full-Duplex, DF1 Half-Duplex Master/ Slave, and ASCII protocols		
	Channel 1	DH-485 protocol			
SLC 5/04	Channel 0		DH-485, DF1 Full-Duplex, DF1 Half-Duplex Master/ Slave, and ASCII protocols		
	Channel 1			DH+ protocol	
SLC 5/05	Channel 0		DH-485, DF1 Full-Duplex, DF1 Half-Duplex Master/ Slave, and ASCII protocols		
	Channel 1				Ethernet TCP/IP protocol

a.A 1761-NET-AIC (or 1747-AIC) is required when connecting to a DH-485 network.

Protocol Options

Ethernet TCP/IP Protocol

Standard Ethernet, utilizing the TCP/IP protocol, is used as the backbone network in many office and industrial buildings. Ethernet is a local area network that provides communication between various devices at 10 Mbps. This network provides the same capabilities as DH+ or DH–485 networks, plus:

- SNMP support for Ethernet network management
- optional dynamic configuration of IP addresses using a BOOTP utility
- SLC 5/05 Ethernet data rate up to 40 times faster than SLC 5/04 DH+ messaging
- ability to message entire SLC 5/05 data files
- much greater number of nodes on a single network possible compared to DH–485 (32) and DH+ (64)

Data Highway Plus (DH+) Protocol

The Data Highway Plus protocol is used by the PLC–5 family of processors and the SLC 5/04 processor. This protocol is similar to DH–485, except that it can support up to 64 devices (nodes) and runs at faster communication (baud) rates.

DH–485 Protocol

The SLC 500 processors have a DH–485 channel that supports the DH–485 communication network. This network is a multi–master, token–passing network protocol capable of supporting up to 32 devices (nodes). This protocol allows:

- monitoring of data and processor status, along with program uploading and downloading of any device on the network from one location
- SLC processors to pass data to each other (peer–to–peer communication)
- operator interface devices on the network to access data from any SLC processor on the network

DF1 Full–Duplex Protocol

DF1 Full–Duplex protocol (also referred to as DF1 point–to–point protocol) allows two devices to communicate with each other at the same time. This protocol allows:

- transmission of information across modems (dial–up, leased line, radio, or direct cable connections)
- communication to occur between Allen–Bradley products and third–party products

DF1 Half–Duplex Protocol (Master and Slave)

DF1 Half–Duplex protocol provides a multi–drop single master/multiple slave network capable of supporting up to 255 devices (nodes). This protocol also provides modem support and is ideal for SCADA (Supervisory Control and Data Acquisition) applications because of the network capability.

ASCII Protocol

The ASCII protocol provides connection to other ASCII devices, such as bar code readers, weigh scales, serial printers, and other intelligent devices.

System Protection Options

The SLC 500 family of processors offer a number of hardware and software security features that allow you to protect your system from unauthorized changes to program or data files. The different types of protection are:

Types of Protection	SLC 5/01	SLC 5/02	SLC 5/03 SLC 5/04 SLC 5/05
Password	•	•	•
Future Access (OEM Lock)	•	•	•
Program Owner	•	•	•
Program Files			•
Data Table Files	•	•	•
Memory Module Data File Overwrite			•
Memory Module Program Compare			•
Memory Module Write Protection			•
Force Protection			•
Keyswitch			•
Communication Channel Protection			

I/O Usages

The SLC 500 family of processors support a variety of I/O modules, allowing you to exactly match your application. The following table lists the various types of I/O modules and their compatibility with the SLC 500 processors.

I/O Module	SLC 5/01	SLC 5/02	SLC 5/03 SLC 5/04 SLC 5/05
1746–Discrete Input/Output AC/DC	•	•	•
1746sc–Isolated Discrete Input/Output AC/DC[a]	•	•	•
1746–Analog Modules	•	•	•
1746sc–Isolated Analog Modules	•	•	•
1746–NT4 and 1746–INT4 Thermocouple Modules and 1746sc–NT8 Isolated Thermocouple Module	•	•	•
1746–NR4 RTD Input Module	•	•	•
1747–SN Remote I/O Scanner Module		•	•
1746–SDN DeviceNet Scanner Module		•	•
1746–BAS Basic Module	•	•	•
1747–KE DH–485/RS232 KE Module	•	•	•
1746–HSCE High–Speed Counter Encoder Module		•	•
1746–HSTP1 Stepper Controller Module		•	•
1746–HS IMC 110 Servo Controller Module	•	•	•
1746–HSRV Servo Control Module			•
1746–QV Open–Loop Velocity Control Module		•	•
1746–BTM Barrel Temperature Module		•	•
1746–QS Synchronized Axes Module		•	•

a. Sold and supported by Spectrum Controls, Inc., Bellevue, WA. For additional information, contact Spectrum at (206) 746-9481.

Programming Instructions

The following programming instructions are used with the SLC 500 processors. Included are instruction execution times (µs) for the processors when the instruction is True and when floating point math is used and the instruction is True.

Basic Instructions

Instruction Mnemonic and Name	Execution Times (µs)				Function - Conditional Instructions Input or Output
	SLC 5/01	SLC 5/02	SLC 5/03	SLC 5/04 SLC 5/05	
XIC Examine if Closed	4	2.4	0.44	0.37	Conditional instruction. True when bit is on (1).
XIO Examine if Open	4	2.4	0.44	0.37	Conditional instruction. True when bit is off (0).
OTE Output Energize	18	11	0.63	0.56	Output instruction. True (1) when conditions preceding it are true. False when conditions preceding it go false.
OTL Output Latch	19	11	0.63	0.56	Output instruction. Addressed bit goes true (1) when conditions preceding the OTL instruction are true. When conditions go false, OTL remains true until the rung containing an OTU instruction with the same address goes true.
OTU Output Unlatch	19	11	0.63	0.56	Output instruction. Addressed bit goes false (0) when conditions preceding the OTU instruction are true. Remains false until the rung containing an OTL instruction with the same address goes true.
OSR One-Shot Rising	34	20	10.80	9.10	Conditional instruction. Makes rung true for one scan upon each false–to–true transition of conditions preceding it in the rung.
TON Timer On-Delay	135	83	1.40	1.31	Counts time intervals when conditions preceding it in the rung are true. Produces an output when accumulated value (count) reaches preset value.
TOF Timer Off-Delay	140	86	1.40	1.31	Counts time intervals when conditions preceding it in the rung are false. Produces an output when accumulated value (count) reaches preset value.
RTO Retentive Timer	140	86	1.40	1.31	This is an On–Delay timer that retains its accumulated value when: • Rung conditions go false. • The mode changes to program from run or test. • The processor loses power. • A fault occurs.
CTU Count Up	111	69	1.40	1.31	Counts up for each false–to–true transition of conditions preceding it in the rung. Produces an output when accumulated value (count) reaches the preset value.
CTD Count Down	111	69	1.40	1.31	Counts down for each false–to–true transition of conditions preceding it in the rung. Produces an output when accumulated value (count) reaches preset value.
RES Reset	40	26	1.40	1.31	Used with timers and counters. When conditions preceding it in the rung are true, the RES instruction resets the accumulated value and control bits of the timer or counter.

Comparison Instructions

Instruction Mnemonic and Name	Execution Times (µs) Floating Point (µs) [a] [b]				Function - Conditional (Input) Instructions
	SLC 5/01	SLC 5/02	SLC 5/03	SLC 5/04 SLC 5/05	
EQU Equal	60	38	1.25/12.94	1.12 / 12.5	Instruction is true when source A = source B.
NEQ Not Equal	60	38	1.25 / 13.25	1.12 / 12.18	Instruction is true when source A =/ source B.
LES Less Than	60	38	1.25 / 13.19	1.12 / 13.94	Instruction is true when source A < source B.
LEQ Less Than or Equal	60	38	1.25 / 13.19	1.12 / 13.93	Instruction is true when source A ≤ source B.
GRT Greater Than	60	38	1.25 / 14.82	1.12 / 12.62	Instruction is true when source A > source B.
GEQ Greater Than or Equal	60	38	1.25 / 14.81	1.12 / 14.31	Instruction is true when source A ≥ source B.
MEQ Masked Comparison for Equal	75	47	38	22.75	Compares 16–bit data of a source address to 16–bit data at a reference address through a mask. If the values match, the instruction is true.
LIM Limit Test	-	45	1.95 / 22.81	1.68 / 20.19	True/false status of the instruction depends on how a test value compares to specified low and high limits.

a.Floating point times do not apply to SLC 5/03 OS300 processors.

b.When only one Execution Time is listed for an instruction, Floating Point does not apply.

Math Instructions

Instruction Mnemonic and Name[a]	Execution Times (µs) Floating Point (µs) [b] [c]				Function - Output Instructions
	SLC 5/01	SLC 5/02	SLC 5/03	SLC 5/04 SLC 5/05	
Add Add	122	76	1.70 / 38.44	1.50 / 18.22	When rung conditions are true, the ADD instruction adds source A to source B and stores the result in the destination.
SUB Subtract	125	77	1.70 / 38.19	1.50 / 19.50	When rung conditions are true, the SUB instruction subtracts source B from source A and stores the result in the destination.
MUL Multiply	230	140	20 / 39.05	17.75 / 21.94	When rung conditions are true, the MUL instruction multiplies source A by source B and stores the result in the destination.
DIV Divide	400	242	23 / 57.56	25.9 / 23.27	When rung conditions are true, the DIV instruction divides source A by source B and stores the result in the destination and the math register.
DDV Double Divide	650	392	33	29.6	When rung conditions are true, the DDV instruction divides the contents of the math register by the source and stores the result in the destination and the math register.
NEG Negate	110	68	1.70 / 12.38	1.5 / 11.87	When rung conditions are true, the NEG instruction changes the sign of the source and places it in the destination.
CLR Clear	40	26	1.70 / 6.62	1.5 / 5.94	When rung conditions are true, the CLR instruction clears the destination to zero.
SQR Square Root	—	162	32.00 / 70.00	28.8 / 18.87	When rung conditions are true, the SQR instruction calculates the square root of the source and places the result in the destination.
SCL Scale	—	480	[d] / 32.00	[d] / 33.06	When rung conditions are true, the SCL instruction multiplies the source by a specified rate. The result is added to an offset value and placed in the destination.
SCP Scale with Parameters	—	—	33.10 / 196.10	29.85 / 94.15	Produces a scaled output value that has a linear relationship between the input and scaled values.
CPT Compute	—	—	[d] / 8.8	[d] / 7.7	Evaluates an expression and stores the result in the destination. To get the total execution time for a CPT instruction, take the CPT execution time plus each additional math instruction execution time, plus the number of math instructions times 3.01. For example if an SLC 5/03 CPT instruction calls one ADD and one SUB instruction, the calculation is: 8.8 + 1.70 + 1.70 + 2(3.01) = 18.22

SWP Swap	—	—	24 + 13.09 per word	22.6 + 12.13 per word	Swaps the low and high bytes of a specified number of words in a bit integer, ASCII, or string file.
ABS Absolute Value	—	—	9.95 / 5.20	8.60 / 4.35	Calculates the absolute value of the source and places the result in the destination.
XPY X to the Power of Y Register/Data	—	—	[d] / 699.30	[d] /335.10	Raises a value to a power and stores the result in the destination.
LOG Log to the Base 10	—	—	[d] / 390.80	[d] / 54.55	Takes the log base 10 of the value in the source and stores the result in the destination.
LN Natural Log	—	—	[d] / 392.00	[d] / 51.35	Takes the natural log of the value in the source and stores it in the destination.
SIN Sine	—	—	[d] / 311.95	[d] / 38.05	Takes the sine of a number and stores the result in the destination.
COS Cosine	—	—	[d] / 310.90	[d] / 37.20	Takes the cosine of a number and stores the result in the destination.
TAN Tangent	—	—	[d] / 406.35	[d] / 43.00	Takes the tangent of a number and stores the result in the destination.
ASN Arc Sine	—	—	[d] / 483.05	[d] / 41.45	Takes the arc sine of a number and stores the result (in radians) in the destination.
ACS Arc Cosine	—	—	[d] / 510.85	[d] / 51.90	Takes the arc cosine of a number and stores the result (in radians) in the destination.
ATN Arc Tangent	—	—	[d] / 387.05	[d] / 40.15	Takes the arc tangent of a number and stores the result (in radians) in the destination.

a.Applies to SLC 5/03 OS302, SLC 5/04 OS401 and SLC 5/05 OS500 processors.

b.Floating point times do not apply to SLC 5/03 OS300 processors.

c.When only one Execution time is listed for an instruction, Floating Point does not apply.

d.The execution times assum floating point data. If signed interger data is used, add 15 microseconds per instruction execution time.

Data Handling Instructions

Instruction Mnemonic and Name	Execution Times (µs) Floating Point (µs) [b] [c]				Function - Output Instructions
	SLC 5/01	SLC 5/02	SLC 5/03	SLC 5/04 SLC 5/05	
TOD Convert to BCD	200	122	38	34.06	When rung conditions are true, the TOD instruction converts the source value to BCD and stores it in the math register or the destination.
FRD Convert from BCD	223	136	31	23.88	When rung conditions are true, the FRD instruction converts a BCD value in the math register or the source to an integer and stores it in the destination.
RAD Degrees to Radians[a]	—	—	[d] / 31.80	[d] / 24.65	When rung conditions are true, RAD converts degrees (source) to radians and stores the result in the destination.
DEG Radians to Degrees [a]	—	—	[d] / 32.80	[d] / 24.70	When rung conditions are true, DEG converts radians (source) to degrees and stores the result in the destination.
DCD Decode	80	50	10	8.88	When rung conditions are true, the DCD instruction decodes 4–bit value (0 to 16), turning on the corresponding bit in 16–bit destination.
COP File Copy	45 + 21 per word	29 + 13 per word	30 + 2.20 per word	20.2 + 2.0 per word	When rung conditions are true, the COP instruction copies a user–defined source file to the destination file.
FLL File Fill	37 + 14 per word	25 + 8 per word	28 + 2 per word	21.9 + 2.5 per word	When rung conditions are true, the FLL instruction loads a source value into specified elements in a user–defined file.
MOV Move	20	14	1.25 / 12.19	1.12 / 11.44	When rung conditions are true, the MOV instruction moves a copy of the source to the destination.
MVM Masked Move	115	71	19	17.40	When rung conditions are true, the MVM instruction moves a copy of the source through a mask to the destination.
AND And	87	55	1.70	1.5	When rung conditions are true, sources A and B of the AND instruction are ANDed and stored in the destination.
OR Inclusive Or	87	55	1.70	1.5	When rung conditions are true, sources A and B of the OR instruction are ORed bit by bit and stored in the destination.
XOR Exclusive Or	87	55	1.70	1.5	When rung conditions are true, sources A and B of the XOR instruction are Exclusive ORed and stored in destination.
NOT Not	66	42	1.70	1.5	When rung conditions are true, the source of the NOT instruction is NOTed bit by bit and stored in the destination.
FFL Load	—	150	58	40.75	First In First Out (FIFO). The FFL instruction loads a word into a FIFO stack on successive false–to–true transitions. The FFU unloads a word from the stack on successive false–to–true transitions. The first word loaded is the first to be unloaded.
FFU Unload	—	150 + 11 per word	79 + 2.20 per word	60 + 2 per word	
LFL Load	—	150	58	40.70	Last In First Out (LIFO). The LFL instruction loads a word into a LIFO stack on successive false–to–true transitions. The LFU unloads a word from the stack on successive false–to–true transitions. The last word loaded is the first to be unloaded.
LFU Unload	—	180	66	34.70	

a.Applies to SLC 5/03 OS302 and SLC 5/04 OS401 processors.

b.Floating point times do not apply to SLC 5/03 OS300 processors.

c.When only one Execution Time is listed for an instruction, Floating Point does not apply.

d.The execution times assum floating point data. If signed integer data is used, add 15 microseconds per instruction execution time.

Program Flow Instructions

Instruction Mnemonic and Name	Execution Times (µs)				Function - Conditional or Output Instructions
	SLC 5/01	SLC 5/02	SLC 5/03	SLC 5/04 SLC 5/05	
JMP Jump to Label	38	23	44.45	37.44	Output instruction. When rung conditions are true, the JMP instruction causes the program scan to jump forward or backward to the corresponding LBL instruction.
LBL Label	2	4	0.25	0.18	This is the target of the correspondingly numbered JMP instruction.
JSR Jump to Subroutine	46	28	131.0	112.0	Output instruction. When rung conditions are true, the JSR instruction causes the processor to jump to the targeted subroutine file.
SBR Subroutine	2	4	0.25	0.18	Placed as first instruction in a subroutine file. Identifies the subroutine file.
RET Return from Subroutine	34	20	23	20.0	Output instruction, placed in subroutine. When rung conditions are true, the RET instruction causes the processor to resume program execution in the main program file or the previous subroutine file.
MCR Master Control Reset	10	6	4	3.0	Output instruction. Used in pairs to inhibit or enable a zone within a ladder program.
TND Temporary End	32	22	12	13.05	Output instruction. When rung conditions are true, the TND instruction stops the program scan, updates I/O, and resumes scanning at rung 0 of the main program file.
SUS Suspend	12	7	12	10.31	Output instruction, used for troubleshooting. When rung conditions are true, the SUS instruction places the controller in the Suspend Idle mode. The suspend ID number is placed in word S:7 and the program file number is placed in S:8.
IIM Immediate Input with Mask	372	340	51.85	51.0	When conditions preceding it in the rung are true, the IIM instruction is enabled and interrupts the program scan to write a word of masked external input data to input data file.
IOM Immediate Output with Mask	475	465	70.90	75.74	When conditions preceding it in the rung are true, the IOM instruction is enabled and interrupts the program scan to read a word of data from the output data file and transfer the data through a mask to the corresponding external outputs.

Application Specific Instructions

Instruction Mnemonic and Name	Execution Times (µs)				Function - Output Instructions
	SLC 5/01	SLC 5/02	SLC 5/03	SLC 5/04 SLC 5/05	
BSL Bit Shift Left **BSR** Bit Shift Right	144 + 24 per word	89 + 14 per word	50 + 2.30 per word	31.5 + 2.31 per word	On each false–to–true transition, these instructions load a data bit into a bit array, shift the pattern of data through the array, and unload the end bit of data. The BSL shifts data to the left and the BSR shifts data to the right.
SQO Sequencer Output	225	137	70	44.1	On each false–to–true transition, these instructions load a data bit into a bit array, shift the pattern of data through the array, and unload the end bit of data. The BSL shifts data to the left and the BSR shifts data to the right.
SQC Sequencer Compare	225	137	60	33.2	On successive false–to–true transitions, the SQC moves a step through the programmed sequencer file, comparing the data through a mask to a source word or file for equality.
SQL Sequencer Load	—	135	56	33.2	On successive false–to–true transitions, the SQL moves a step through the sequencer file, loading a word of source data into the current element of the sequencer file.

Communication Instructions

Instruction Mnemonic and Name	Execution Times (µs)				Function - Output Instructions
	SLC 5/01	SLC 5/02	SLC 5/03	SLC 5/04 SLC 5/05	
MSG Message Read/ Write	—	180	203	183	This instruction transfers data from one node to another on the communication network. When the instruction is enabled, message transfer is pending. Actual data transfer takes place at the end of the scan.
SVC Service Communications	—	240	240	200	When conditions preceding it in the rung are true, the SVC instruction interrupts the program scan to execute the service communication portion of the operating cycle.

Proportional Integral Derivative Instruction

Instruction Mnemonic and Name	Execution Times (µs)				Function - Output Instructions
	SLC 5/01	SLC 5/02	SLC 5/03	SLC 5/04 SLC 5/05	
PID Proportional Integral Derivative	—	3600	272	169.82	This instruction is used to control physical properties such as temperature, pressure, liquid level, or flow rate of process loops.

ASCII Instructions

Instruction Mnemonic and Name[a]	Execution Times (µs)		Function - Output Instructions
	SLC 5/03	SLC 5/04 SLC 5/05	
ABL Test Buffer for Line	129.9	156.0	Determines the number of characters in the buffer, up to and including the end–of–line characters (termination).
ACB Number of Characters in Buffer	140.7	131.0	Determines the total characters in the buffer.
ACI String to Integer	86.62	56.0	Converts an ACSII string to an integer value.
ACL ASCII Clear Receive and/or Send Buffer	367.5	332.8	Clears the ASCII buffer.
ACN String Concantenate	69.4 + 2.1 per character	56 + 2.5 per character	Combines two strings using ACSII strings as operands.
AEX String Extract	56.2 + 4.7 per character	43.4 + 4.0 per character	Creates a new string by taking a portion of an existing string and linking it to a new string.
AHL ASCII Handshake Lines	138.7	115.1	Sets or resets the RS-232 Data Terminal REady and Request to Sender handshake control lines for the modem.
AIC Integer to String	103.4	110.0	Converts an integer value to an ASCII string.
ARD ASCII Read Characters	181.8	151.0	Reads characters from the buffer and stores them in a string.
ARL ASCII Read Line	190.0	156.0	Reads characters from the buffer up to and including the end-of-line characters and stores them in a string.
ASC String Search	53.4 + 1.8 per character	43.5 + 2.5 per character	Searches an existing string for an occurrence of the source string.
ASR ASCII String Compare	49.69	43.5	Compares two ASCII strings.
AWA ASCII Write with Append	365.5	307.8	Adds the two appended characters set from the ASCII configuration menu.
AWT ASCII Write	263.8	217.3	Writes characters from a source string to a display device.

a.Only SLC 5/03 (OS301, OS302), SLC 5/04 and SLC 5/05 processors use these instructions.

Interrupt Routine Instructions

Instruction Mnemonic and Name	Execution Times (µs)				Function - Output Instructions
	SLC 5/01	SLC 5/02	SLC 5/03	SLC 5/04 SLC 5/05	
STD Selectable Timed Disable	—	9	4	3.56	Associated with the Selectable Timed Interrupt function. STD and STE are used to prevent an STI from occurring during a portion of the program; STS initiates an STI.
STE Selectable Timed Enable	—	9	5	5.0	
STS Selectable Timed Start	—	72	58	44.38	
IIE I/O Interrupt Enable	—	42	16	10.44	The IIE, IID and RPI instructions are used with specialty I/O modules capable of generating an I/O interrupt.
IID I/O Interrupt Disable	—	39	6	5.81	
RPI Reset Pending I/O Interrupt	—	240	78 + 60 per added slot	91 + 56 per added slot	
REF I/O Refresh	—	240	240	200	When conditions preceding it in the rung are true, the REF instruction interrupts the program scan to execute the I/O scan (write outputs-service comms-read inputs). The program scan then resumes.
INT Interrupt Subroutine	—	0	0.25	0.18	Associated with STI interrupts and I/O event-driven interrupts.

Indirect Addressing

The following sections describe how indirect addressing affects the execution time of instructions in the SLC 5/03 OS302, SLC 5/04 OS401, and SLC 5/05 processors. The timing for an indirect address is affected by:

- the form of the indirect address
- if the indirect address is a source or destination parameter
- whether indirect addressing is used in either a COP, FLL, FFL/FFU, LFL/LFU, BSR, BSL, or MVM instruction
- whether indirect addressing is used in either an XIC, XIO, OTU, OTL, OTE, or OSR instruction

For the address forms in the table on the next page, you can substitute the following file types:

For an Integer (N)	For a String (ST)
Input (I)	Control (R)
Output (O)	Counter (C)
Bit (B)	Timer (T)
Floating Point (F)	
ASCII (A)	

Execution Times for Word–Level Indirect Addresses

For most types of instructions that contain an indirect address(es), look up the form of the indirect address in the table below and add that time to the execution time of the instruction.

Address Form[a]	Source Operand (µs)		Destination Operand (µs)		If used in a file type instruction	
	SLC 5/03	SLC 5/04 SLC 5/05	SLC 5/03	SLC 5/04 SLC 5/05	SLC 5/03	SLC 5/04 SLC 5/05
N7:[*]	65.1	56.15	63.10	54.20	76.35	66.75
ST12:[*].[*]	69.45	60.00	67.45	58.05	80.70	70.60
ST12:[*].0	74.65	59.60	72.65	57.65	85.90	70.20
ST12:0.[*]	74.65	59.60	72.65	57.65	85.90	70.20
N[*]:[]:[	105.90	89.40	131.50	112.55	138.75	118.70
N[*]:0	111.10	89.00	136.70	112.15	143.95	118.30
N[*]:0	111.10	89.00	136.70	112.15	143.95	118.30
ST[*]:[*].[*]	110.25	93.25	135.85	116.40	143.10	122.55
ST[*]:[*].0	115.45	92.85	141.05	116.00	148.30	122.15
ST[*]:0.[*]	115.45	92.85	141.05	116.00	148.30	122.15
ST[*]:0.0	120.65	92.45	146.25	115.60	153.50	121.75
#N7:[*]	73.05	59.35	64.65	57.30	86.80	69.80
#ST12:[*].[*]	77.40	63.20	69.00	61.15	91.15	73.65
#ST12:[*].0	82.60	62.80	74.20	60.75	96.35	73.25
#ST12:0.[*]	82.60	62.80	74.20	60.75	96.35	73.25
#N[*]:[*]	110.95	92.95	133.40	114.40	146.65	121.35
#N[*]:0	116.15	92.55	138.60	114.00	151.85	120.95
#ST[*]:[*].[*]	115.30	96.80	137.75	118.25	151.00	125.20
#ST[*]:[*].0	120.50	96.40	142.95	117.85	156.20	124.80
#ST[*]:0.[*]	120.50	96.40	142.95	117.85	156.20	124.80
#ST[*]:0.0	125.70	96.00	148.15	117.45	161.40	124.40

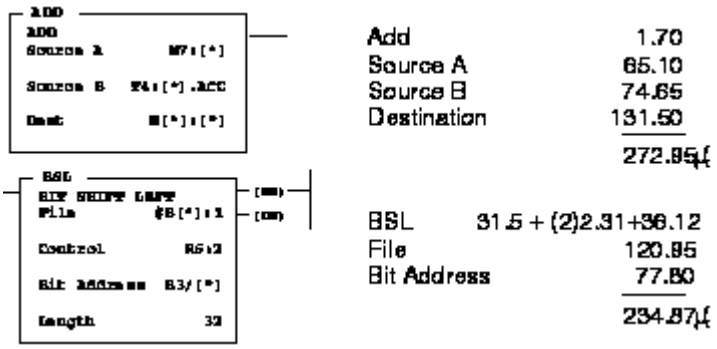
a.[*] indicates that an indirect reference is substituted.

Execution Times for Bit–Level Indirect Addresses

Indirect bit addresses are based on the form of the indirect address and the type of bit instruction. Use the following two tables to calculate the execution time of a bit instruction.

Address Form	Additional Time (µs)	
	SLC 5/03	SLC 5/04 SLC 5/05
B3/[*]	96.70	77.80
B3:1/[*]	96.70	77.80
B3:[*=/]:[	91.50	72.80
ST12:[*].[*=/]:[	100.65	76.65
ST12:[*].[*]/0	100.85	76.25
ST12:[*].0/[*]	100.85	76.25
ST12:[*].0/0	105.85	75.85
ST12:0.[*] /0	105.85	75.85
ST12:0.0/[*]	105.85	75.85
B[*=/]:[	171.50	141.40
B[*]:1/[*]	171.50	141.40
B[*]:[*=/]:[	166.30	141.80
ST[*]:[*].[*=/]:[	170.65	145.65
ST[*]:[*].[*]/0	175.85	145.25
ST[*]:[*].0/[*]	175.85	145.25
ST[*]:[*].0/0	181.05	144.85
ST[*]:0.[*=/]:[	175.85	145.25
ST[*]:0.[*]/0	181.05	144.85
ST[*]:0.0/[*]	181.05	144.85
ST[*]:0.0/0	186.25	144.45

Execution Time Examples - Word Level and Bit Level Indirect Address



Instruction Execution Times

Instruction	Execution Time (µs)	
	SLC 5/03	SLC 5/04 SLC 5/05
XIC	10.20	8.72
XIO	14.65	12.76
OTU	6.30	5.45
OTL	9.35	5.40
OTE	6.25	5.50
OSR	10.50	8.10

Execution Time Example - Bit Instruction Using an Indirect Address

To calculate the execution time of an XIC at B3/[N7:0] using an SLC 5/03 processor add the following:

Execution Time for Bit–Level Indirect Address + Instruction Execution Time =10.20 + 96.70 = 106.90

Specifications

The following table summarizes the detailed specifications for the SLC 500 processor family:

Specification	SLC 5/01	SLC 5/02	SLC 5/03	SLC 5/04	SLC 5/05
	1747–L511 1747–L514	1747–L524	1747–L531 1747–L532	1747–L541 1747–L542 1747–L543	1747–L551 1747–L552 1747–L553
Memory Size (words)	1K (1747–L511) 4K (1747–L514)	4K	8K (1747–L531) 16K (1747–L532)	16K (1747–L541) 32K (1747–L542) 64K (1747–L543)	16K (1747–L551) 32K (1747–L552) 64K (1747–L553)
Max. I/O Capacity	3940 Discrete	4096 Discrete	4096 Discrete	4096 Discrete	4096 Discrete
Max. Local Chassis/Slots	3/30	3/30	3/30	3/30	3/30
Programming	•RSLogix 500 (V1.00 or later), SLC–500 A.I. Series •APS Programming Software •HHT		**1747–L531:** •RSLogix 500 (V1.26.03 or later) •SLC 500 A.I. Series (V8.15 or later) **1747–L532:** •RSLogix 500 (V1.24.04 or later) •SLC 500 A.I. Series (V8.10 or later) •APS (V6.0 or later)	•RSLogix 500 (V1.24.04 or later) •SLC 500 A.I. Series (V8.10 or later) •APS (V6.0 or later)	•RSLogix 500 (V2.10 or later)
Programming Instructions	52	71	99	99	99
Typical Scan Time[a]	8 ms/K	4.8 ms/K	1 ms/K	0.9 ms/K	0.9 ms/K
Bit Execution (XIC)	4 µs	2.4 µs	0.44 µs	0.37 µs	0.37 µs

a.The scan times are typical for a 1K ladder logic program consisting of simple ladder logic and communication servicing. Actual scan times depend onyour program size, instructions used and the communication protocol.

The following table summarizes the communication options for the SLC 500 processor family.

Communications Protocol	Processor				
	SLC 5/01	SLC 5/02	SLC 5/03	SLC 5/04	SLC 5/05
DH485 peer–to–peer	receive only	receive and initiate	receive and initiate		
DH485 via RS232 port			receive and initiate[c]	receive and initiate[c]	receive and initiate[c]
DF1 via RS232 port (full–duplex or half–duplex master or slave)	receive only[a]	receive only[a]	receive and initiate	receive and initiate	receive and initiate
ASCII via RS232 port			receive and initiate	receive and initiate	receive and initiate
Data Highway Plus (DH+)	receive only[b]	receive only[b]	receive and initiate[d]	receive and initiate	receive and initiate
Ethernet					receive and initiate

a.A 1747-KE or 1770-KF3 is required to bridge from DF1 (full-duplex or half-duplex slave only) to DH485.

b.A 1785-KA5 is required to bridge from HD+ to DH485.

c.If using 1747-AIC for isolation, connect to DH-485 network using 1747-PIC; if using 1761-NET-AIC for isolation, directly connect to DH-485 network with 1747-CP3 serial cable (or equivalent RS-232 null-modem cable).

d.Either a 1785-KA5 is required to bridge from DH+ to DH485 or the SLC 5/04's channel-to-channel passthru feature may be used to bridge between DH+ and DH485 or between DH+ and DF1 Full-Duplex (DH+ to DF1 Full-Duplex passthru available starting with OS401). Another option is to use the 1785-KE to bridge between DH+ and DF1 Full-Duplex or DH+ and a DF1 Half-Duplex Master/Slave network.

Note: The 1785-KA5 and 1785-KE modules require use of a 1771-series chassis and power supply.

The following table summarizes the general specifications for the SLC 500 processor family:

Description		Specification
Power Supply Loading	SLC 5/01 and SLC 5/02	350mA at 5V dc. 105 mA at 24V dc
	SLC 5/03	500 mA at 5V dc. 175 mA at 24V dc
	SLC 5/04 and SLC 5/05	1.0 A at 5V dc 200 mA at 24V dc
Program Scan Hold-up time after Loss of Power		20 ms to 3 s (dependent on power supply loading)
Clock/Calendar Accuracy (Applicable only to SLC 5/03, SLC 5/04, and SLC 5/05 processors)		±54 sec/month at +25° C (77° F) ±81 sec/month @ +60° C (+140°F)
Noise Immunity		NEMA Standard ICS 2-230
Vibration	Displacement	0.015 inch, peak-to-peak at 5-57 Hz
	Acceleration	2.5Gs at 57-2000 Hz
Shock (operating)		30Gs
Ambient Temperature Rating	Operating Temperature	0 to +60°C (+32°F to +140°F)
	Storage Temperature	-40°C to +85°C (-40°F to 185°F)
Humidity		5 to 95% without condensation
Certification		UL listed CSA approved Class 1, Groups A, B, C or D, Division 2 CE compliant for all applicable directives

The following table summarizes the available memory back up options for the SLC 500 processors. EEPROM and UVPROM memory modules provide non-volatile memory backup. Flash EPROMs (Flash Erasable Programmable Read-Only Memory) combine the versatility of EEPROMs with the security of UVPROMs.

Specification	SLC 5/01	SLC 5/02	SLC 5/03	SLC 5/04	SLC 5/05
	1747-L511 1747-L514	**1747-L524**	**1747-L531 1747-L532**	**1747-L541 1747-L542 1747-L543**	**1747-L551 1747-L552 1747-L553**
EEPROM	1747-M1 1747-M2	1747-M2			
UVPROM	1747-M3 1747-M4	1747-M4			
Flash			1747-M11 1747-M12 (OS302 or later)	1747-M11 1747-M12 (OS401 or later)	1747-M11 1747-M12

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